Evaluation of the LDC Computing Platform for Point 2
SuperMicro X6DHE-XB, X7DB8+

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ALICE DAQ
CERN
10 October 2006
Purpose

- **Background:**
  - Test the machine (X6DHE-XB) as LDC with 6 D-RORCs

- **Machines:**
  - Elonex: Supermicro X7DB8+(2x Intel dual core Xeon)
  - Elonex: Supermicro X6DHE-XB (2x Intel Xeon)

- **Evaluation program:**
  - Linux installation
  - DATE V5 installation
  - D-RORC throughput with DATE
  - Perform a range of runs with internal D-RORC generator and receiving through DATE
  - Quick comparison of two machines based on mentioned motherboards.
Supermicro X6DHE-XB

<table>
<thead>
<tr>
<th>CPU</th>
<th>2x Xeon 2.8 GHz, 2 MB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chipset</td>
<td>E7520</td>
</tr>
<tr>
<td>FSB</td>
<td>800 MHz</td>
</tr>
<tr>
<td>Memory</td>
<td>4 GB (max 16GB), DDR 333</td>
</tr>
<tr>
<td>I/O</td>
<td>2x PCI-X (64/133)</td>
</tr>
<tr>
<td></td>
<td>4x PCI-X (64/100)</td>
</tr>
<tr>
<td></td>
<td>1x PCI-e (x4)</td>
</tr>
<tr>
<td>Network</td>
<td>2x GbE, BCM5721</td>
</tr>
<tr>
<td>Disk</td>
<td>74 GB, SATA</td>
</tr>
<tr>
<td>Graphics</td>
<td>Rage XL 8 MB</td>
</tr>
<tr>
<td>Periphery</td>
<td>2x USB front, 2x USB back Serial, PS/2</td>
</tr>
<tr>
<td>Chassis</td>
<td>4U, 1x 550W</td>
</tr>
</tbody>
</table>

Testing the machine (X6DHE-XB) with 6 D-RORCs, X7DB8+
Software Installation

- **Linux**
  - SLC4.3 with kernel 2.6.9-42.0.2.EL.cernsmp
    - no specific problems but X7DB8+, USB boot successful, BIOS ok
  - To use D-RORC modules the BIOS setting needed to be changed: all PCI slots were set to 100 MHz

- **DATE 5.21 installation**
  - MySql
  - mysqltcl
  - BWidt
  - SMI
  - DIM
  - Drivers: rorc and physmem

  have been installed as rpm with additional scripts:
  DATE_basic_Install-SLC4x.bash, DATE_User_Install-SLC4x.bash, DATE_DriversInstall.bash

- **No specific problems**
Common info about measurement

- Total main memory volume = 4 GB
  - 1 GB for Linux (in /etc/grub.conf)
  - other 3 GB for physmem
- SLC 4.3, Kernel 2.6.9-42.0.2.EL.1.cernsmp
- 6 cards D-RORC rev 4 (internal data generator).
- All measurement were done with DATE 5.21. No received event data were recorded to HD. The data from the database were analyzed with scripts. The pictures were built up with gnuplot.
- In total there were performed 390 measurement runs. Because the figures (rates, bandwidth) are fluctuating every run was continued at least 5 minutes.
- Two points on the further graphs: random event size with max=10**4 and max=10**6 Bytes were measured during two days each.
- All measurements with randomly distributed event size were performed with event checking in DATE.
- D-RORC Page Size was 1.5*10**5 Bytes.
Example of editDb for the cards

Testing the machine (X6DHE-XB) with 6 D-RORCs, X7DB8+
Testing the machine (X6DHE-XB) with 6 D-RORCs, X7DB8+

Architecture
One D-RORC card: readout event rate

Event rate of readout from internal D-RORC rev4 generator
(motherboard SuperMicro X6DHE-XB)
[Compiled RORC sw version: v5.1.3/Firmware Version: 2.3/release date=11Jul2006]

Event rate (1/s)

Fixed event fragment size (KB)

size=10**6
rate=390 1/s

28/09/06 17:22
One D-RORC card: Bandwidth of readout

Fixed event fragment size

Bandwidth of readout from internal D-RORC rev4 generator
(Motherboard SuperMicro X6DHE-XB)
[Compiled RORC sw version: v5.1.3/Firmware Version: 2.3/release date=11Jul2006]

Bandwidth (MB/s)

Fixed event fragment size (KB)

28/09/06 17:05
Multiple D-RORC cards: Readout Event rate

Event rate of readout from internal D-RORC rev4 generator
(motherboard SuperMicro X6DHE-XB)
[Compiled RORC sw version: v5.1.3/Firmware Version: 2.3/release date=11Jul2006]

Event rate (l/s)

<table>
<thead>
<tr>
<th>Fixed event fragment size (KB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 card</td>
</tr>
<tr>
<td>2 cards</td>
</tr>
<tr>
<td>3 cards</td>
</tr>
<tr>
<td>4 cards</td>
</tr>
<tr>
<td>5 cards</td>
</tr>
<tr>
<td>6 cards</td>
</tr>
</tbody>
</table>

26/09/06 09:32
Multiple D-RORC cards: Bandwidth of readout

Bandwidth of readout from internal D-RORC rev4 generator
(Motherboard SuperMicro X6DHE-XB)
[Compiled RORC sw version: v5.1.3/Firmware Version: 2.3/release date=11Jul2006]

Fixed event fragment size

Bandwidth (MB/s)

Fixed event fragment size (KB)

26/09/06 09:53

Testing the machine (X6DHE-XB) with 6 D-RORCs, X7DB8+
6xD-RORC cards: Readout Event rate

Event rate of readout from internal D-RORC rev4 generator (motherboard SuperMicro X6DHE-XB)

[Compiled RORC sw version: v5.1.3/Firmware Version: 2.3/release date=11Jul2006]

Random event fragment size

Marked points have been tested two days each

26/09/06 14:35

Testing the machine (X6DHE-XB) with 6 D-RORCs, X7DB8+
6xD-RORC cards: Bandwidth readout

Bandwidth of readout from internal D-RORC rev4 generator
(Motherboard SuperMicro X6DHE-XB)
[Compiled RORC sw version: v5.1.3/Firmware Version: 2.3/release date=11Jul2006]

Marked points have been tested two days each.
Event rate: Influence of D-RORC page size

Event rate of readout from internal D-RORC rev4 generator
six cards; random size 200-1000000 Bytes
(motherboard SuperMicro X6DHE-XB)
[Compiled RORC sw version: v5.1.3/Firmware Version: 2.3/release date=11Jul2006]

6 x D-RORC cards
Random event fragment size
Max size = 10**6 bytes
Bandwidth: Influence of D-RORC page size

Bandwidth of readout from internal D-RORC rev4 generator
six cards; random size 200-1000000 Bytes
(Motherboard SuperMicro X6DHE-XB)
[Compiled RORC sw version: v5.1.3/Firmware Version: 2.3/release date=11Jul2006]

6 x D-RORC cards
Random event fragment size
Max size = 10**6 bytes
## Test of Dual-Core Supermicro X7DB8+

<table>
<thead>
<tr>
<th>Component</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CPU</strong></td>
<td>2 x Xeon LGA 771 pins (Dempsey)</td>
</tr>
<tr>
<td></td>
<td>dual core, cache - total 4 MB</td>
</tr>
<tr>
<td><strong>Chipset</strong></td>
<td>Intel 5000P (BlackFord)</td>
</tr>
<tr>
<td><strong>FSB</strong></td>
<td>1066 MHz</td>
</tr>
<tr>
<td><strong>Memory</strong></td>
<td>4 GB (max 64GB), 667/533 MHz, DDR2</td>
</tr>
<tr>
<td><strong>I/O</strong></td>
<td>2x PCI-Express slots (2x X8; 1x X4)</td>
</tr>
<tr>
<td></td>
<td>3x PCI-X (1x 64/100; 2x 64/133)</td>
</tr>
<tr>
<td></td>
<td>1x PCI-e (x4) SIMLP IPMI 2.0</td>
</tr>
<tr>
<td><strong>Network</strong></td>
<td>2x GbE, BCM5721</td>
</tr>
<tr>
<td><strong>Disk</strong></td>
<td>120 GB, SATA</td>
</tr>
<tr>
<td><strong>Graphics</strong></td>
<td>Rage XL 8 MB</td>
</tr>
<tr>
<td><strong>Periphery</strong></td>
<td>2x USB front, 2x USB back</td>
</tr>
<tr>
<td></td>
<td>Serial, PS/2</td>
</tr>
<tr>
<td><strong>Chassis</strong></td>
<td>5U, 1350W PSU 3+ 1</td>
</tr>
</tbody>
</table>

10 Oct 2006

Testing the machine (X6DHE-XB) with 6 D-RORCs, X7DB8+
## X6DHE-XB vs X7DB8+

<table>
<thead>
<tr>
<th></th>
<th>X6DHE-XB</th>
<th></th>
<th>X7DB8+</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CPU</strong></td>
<td>2x Xeon 2.8 GHz, 1 MB</td>
<td>CPU</td>
<td>2x Xeon LGA 771 (Dempsey) <strong>dual core</strong>, 2.33 GHz, 4 MB</td>
</tr>
<tr>
<td>Chipset</td>
<td>E7520</td>
<td>Chipset</td>
<td>Intel 5000P (BlackFord)</td>
</tr>
<tr>
<td>FSB</td>
<td>800 MHz</td>
<td>FSB</td>
<td>1066 MHz</td>
</tr>
<tr>
<td>Memory</td>
<td>4 GB, DDR 333</td>
<td>Memory</td>
<td>4 GB, DDR2 533 MHz</td>
</tr>
<tr>
<td>I/O</td>
<td>2x PCI-X (64/133) 4x PCI-X (64/100) 1x PCI-e (x4)</td>
<td>I/O</td>
<td>2x PCI-Express slots (2x X8;1x X4) 3x PCI-X (1x 64/100; 2x 64/133) 1x PCI-e (x4) SIMLP IPMI 2.0</td>
</tr>
<tr>
<td>Network</td>
<td>2x GbE, BCM5721</td>
<td>Network</td>
<td>2x GbE, BCM5721</td>
</tr>
<tr>
<td>Memory bandwidth (mem2mem)</td>
<td>1.5 GB/s</td>
<td>Memory bandwidth (mem2mem)</td>
<td>3.8 GB/s</td>
</tr>
</tbody>
</table>

Testing the machine (X6DHE-XB) with 6 D-RORCs, X7DB8+
Recommendation and conclusion

- **Recommendation**: if you need to allocate D-RORC cards in the machine and like to have maximum bandwidth for X6DHE-XB:
  - it is better to avoid to use PCI slot 1 & PCI slot 2 at the same time for high bandwidth information sources.

- **Conclusion**
  - In the test it was shown bandwidth (1.6 GB/sec) when all 6 D-RORC cards are in operation and event fragment size is more $10^{**5}$ bytes.
  - Randomly distributed event fragment size with maximum $10^{**6}$ bytes gives total bandwidth 814 MB/sec during two days run.
  - The machine **X6DHE-XB** is excellent to be used as LDC with 6 D-RORC cards. Selected a single-core LDC for the ALICE DAQ
  - The machine **X7DB8+** might also be used as LDC with max 3 D-RORC cards. First test of a dual-core LDC from Supermicro. Only 3 PCI-X slots. The 6 slots version will be tested when available.
Thank you!

Klaus Schossmaier, Sylvain Chapeland, Ulrich Fuchs and other crew of the PH/AID