## CROS-3B – COORDINATE READOUT SYSTEM (NEW DRIFT CHAMBER VERSION)

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The Radio Electronics Laboratory of the High Energy Physics Division of PNPI continues developing a series of Coordinate ReadOut Systems – the so called CROS-3 series, which was first described in [1] and consists of 3 types of cards: Digitizer, Concentrator and System Buffer. Here we present the CROS-3B version targeted for instrumentation of large-size Drift Chambers (DCs) built at PNPI and designed for using as a tracking detector of the magnetic forward spectrometer for the BGO-OD experiment [2] at the Electron Stretcher Accelerator (ELSA) [3] facility at the Physics Institute of the University of Bonn, Germany.

The CROS-3B retains common features of the CROS-3 series.

- The CROS-3 basic setup consists (see Fig. 1) of 3 types of cards: System Buffer, Concentrator and Digitizer. The cards make use of high-speed serial 2.0 Gb/s fiber and 100 Mb/s copper links to transfer control, trigger and readout data. The cards functionality is based on a firmware loaded into FPGAs.
- The System Buffer provides interfaces to the host computer and trigger logic.
- The Concentrator collects event fragments from the Digitizers in parallel, builds an event and sends it to the System Buffer.
- The Digitizer amplifies, discriminates and continuously digitizes input signals, stores data in the digital pipeline for the trigger decision time and encodes arrival time and positions of hits in a programmable readout gate upon receiving a trigger.

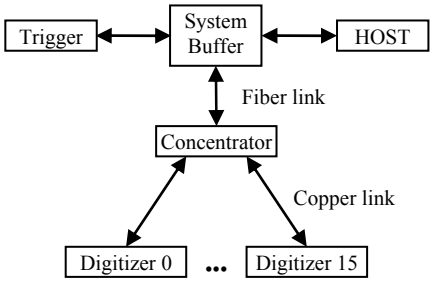


**Fig. 1.** CROS-3 basic setup

There are new features, specific only to the CROS-3B version. The amplifier input impedance and integration constant are optimized to get the best possible time resolution for large-size DCs with a rather big wire capacitance. The system setup is extended by adding a Low-Level Concentrator. So, the System Buffer is now able to control and collect data from up to 4096 channels, 16 times more channels than before. The built-in error detection logic allows to terminate gracefully the readout process in case of hardware failures.

### 1. Drift chambers

PNPI has designed and built 8 DCs for the BGO-OD experiment. The DCs will be used for tracking of charged particles behind a spectrometer magnet. They are grouped into 2 stations. Each station consists of 4 (*X*, *Y*, *U*, and *V*) DCs with sensitive areas of approximately $1.2 \times 2.4$ m$^2$, $1.3 \times 2.4$ m$^2$, $1.8 \times 2.7$ m$^2$, and $1.8 \times 2.7$ m$^2$. All chambers feature similar design and contain a double layer of hexagonal drift cells as shown in Fig. 2, where black dots are sense (anode) wires and white dots are field (cathode) wires. Sense wires are spaced at 17 mm, so the maximum drift distance for tracks perpendicular to the chamber plane (vertical tracks in Fig. 2) is about 8.5 mm. The chambers operate with the standard 70/30 Ar/$CO_2$ gas mixture. The high voltage of –(2.9÷3.2) kV is applied to cathode wires, anode wires being at 0 V for the signal readout.

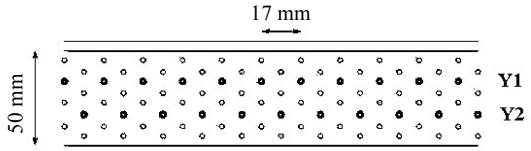


**Fig. 2.** Drift Chamber cell structure, sense wires are shown as black dots, and field wires – as white dots

The *X*, *Y*, *U*, and *V* chambers have 160, 288, 320, and 320 sense wires correspondingly, totaling to 2176 sense wires for the entire system of two stations. The space resolution requirement for the experiment is 300 μm, the trigger rate being about 1 kHz.

### 2. Amplifier optimization

The basic amplifier structure shown in Fig. 3 was used as a starting point for optimization. The structure features 3 independent, but equal, RC circuits that integrate the input current signal *I*. The first trans-impedance amplifier stage $K_R$ is implemented as a common base transistor with low input noise. The amplifier input impedance (including a protection circuit) and the sense wire impedance are well matched.

The second stage $K_V$ is a voltage amplifier with the 500 MHz bandwidth. *D* stands for a differential discriminator with a threshold voltage TH applied to its positive input and an amplified and integrated input signal to its negative input. The goal of the optimization was to choose the RC time constant that would result in the best time/space resolution for the given cell geometry.

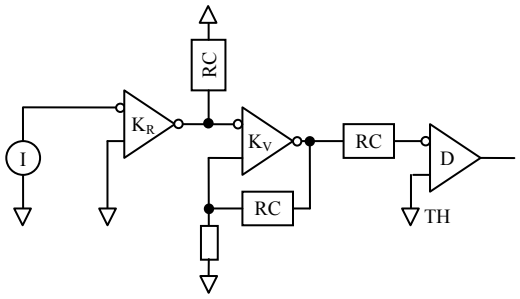


**Fig. 3.** Basic amplifier structure

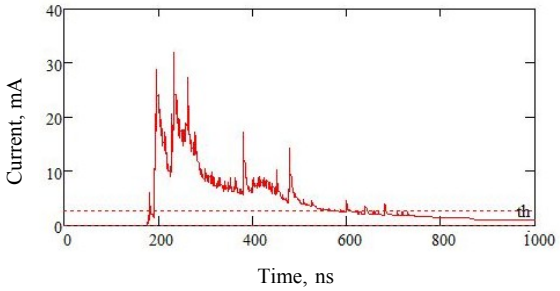


**Fig. 4.** Drift chamber anode current produced by a track

The DC model used assumes each primary electron in the track is independently amplified by a random factor distributed exponentially [4]. Figure 4 shows an example of the anode current produced by a charged particle which traversed the drift cell perpendicular to the chamber plane. The tracks were generated using HEED [5], a program that computes in detail the energy loss of fast charged particles in gases. The simulated tracks in turn were used in GARFIELD [6] to calculate drift times of electrons or, in other words, the arrival time of amplifier input signals.

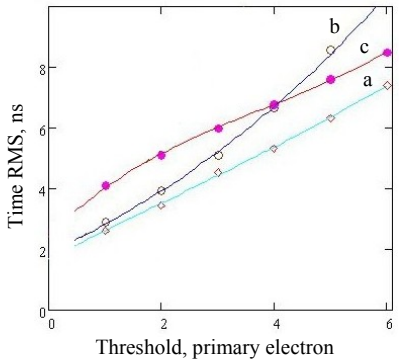


**Fig. 5.** Calculated DC time resolution for the amplifier with: the response as a step function (curve a); 2 ns time constant (curve b); 10 ns time constant (curve c)

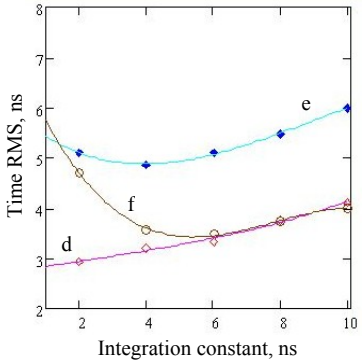


**Fig. 6.** Calculated DC time resolution at the threshold set to: 1 primary electron (curve d); 3 primary electrons (curve e); 5σ (curve f), where σ – noise standard deviation

Figure 5 demonstrates the calculated DC time resolution as a function of the threshold for 3 different ways of processing the anode signal. Ideally, an amplifier with the response as a step function for each primary electron (curve a) gives the best time resolution, which can be called an intrinsic DC resolution. 2 other curves are for the basic amplifier structure with 3 independent integration circuits. The time constant of each circuit is either 2 ns (curve b) or 10 ns (curve c). The smaller time constant is preferred for lower thresholds, while for thresholds above 4 primary electrons the bigger time constant yields better resolution.

The calculated DC time resolution as a function of the integration constant for different threshold settings is presented in Fig. 6. There is almost a linear dependence for 1 primary electron threshold (curve d). At the threshold of 3 primary electrons the best resolution is achieved with the integration constant of 4 ns (curve e). However, both curves do not take into account the input noise of the amplifier. If it is taken into account, the dependence has a distinct minimum at 6 ns for the threshold equal to 5 standard deviations of the input noise (curve f). So, the integration time constant of 6 ns was chosen.

Figure 7 demonstrates the calculated DC space resolution as a function of the track distance from an anode wire at the threshold set to 1 primary electron for an amplifier with the response as a step function (curve g) and for the implemented amplifier (curve h). The space resolution in the second case is only slightly worse than in the first one. The average space resolution is better than the required 300 μm.

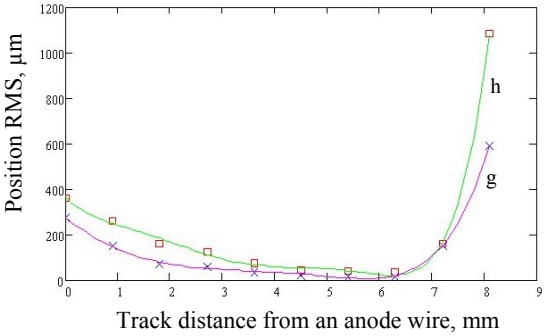


**Fig. 7.** Calculated DC space resolution at the threshold set to 1 primary electron for: an amplifier with the response as a step function (curve g); the implemented amplifier (curve h)

## 3. CROS-3 extended setup

An evaluation of the data payload for copper and fiber data links under the expected occupancy and the trigger rate for the BGO-OD experiment revealed a possibility of merging more data into a single data stream by implementing a setup with 2 Concentrator levels.

A newly developed CROS-3 extended setup, shown in Fig. 8, consists of the same 3 types of cards: System Buffer, Concentrator and Digitizer, but there are two kinds of Concentrators. The regular Concentrator interfaces with the System Buffer over a fiber link as it does in the CROS-3 basic setup. But now, instead of Digitizers, it serves up to 16 Branches consisting of a Low-Level Concentrator with up to 16 Digitizers linked to it. 1 Branch serves an *X* DC, and 2 Branches serve *Y*, *U*, and *V* DCs, the total number of Branches being 14 for the entire system. Each Low-Level Concentrator interfaces with the upstream Concentrator over a copper link. Both Concentrators utilize the same printed circuit board. Though, the boards are differently stuffed and run under different firmwares. The CROS-3 extended setup retains the backward firmware and program compatibility with the CROS-3 basic setup, but serves up to 16 times more channels than before.

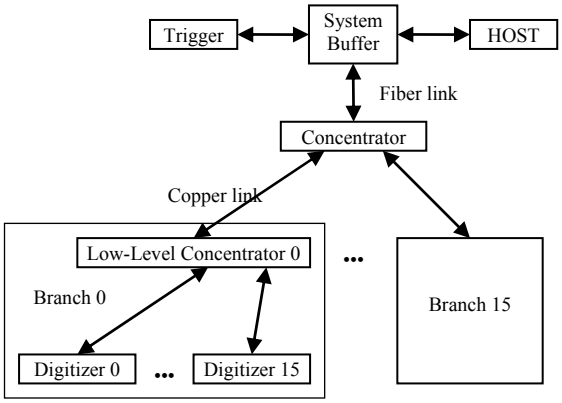


**Fig. 8.** CROS-3 extended setup

## 4. CROS-3B features

The CROS-3B version makes use of the extended setup and includes the following cards:

- CSB-B as the System Buffer, Fig. 9;
- CCB16-B as the Concentrator, Fig. 10;
- CCB10-B as the Low-Level Concentrator, Fig. 11;
- AD16-B as the Digitizer, Fig. 12.

The CSB-B complies with the PCI/PCI-X Local Bus Specifications and supports linear burst reads. The CCB10-B is a ten-port version of the sixteen-port CCB16-B card. The built-in error detection logic can be activated in the CSB-B, CCB16-B, and CCB10-B cards. It gracefully terminates the readout and reports the encountered problem(s) to the HOST in case of the hardware failure.

The AD16-B main features are:

- 16 input channels;
- an effective digitization frequency of 400 MHz or 2.5 ns per time bin;
- an 8-bit programmable threshold;
- an 8-bit programmable pipeline delay in 10 ns steps;
- an 8-bit programmable gate width with 2.5, 5, 10, or 20 ns programmable binning;
- 4 modes of operation with different output formats:
  - in the “Leading-Edge Raw” mode a 2-dimensional array (time bin #, channel #) of the leading edge transitions (hits) of the discriminator outputs is returned;

– in the “Leading-Edge Encoded” mode a list of encoded hits (time bin #, channel #) is returned;
– in the “Time-Over-Threshold” mode a 2-dimensional array (time bin #, channel #) of the discriminator outputs is returned;
– in the “Threshold Curve” mode a threshold scan is performed. For each channel at each step a sum of noise and test pulse hits is counted up, and an array of counter values is returned. The initial threshold, the threshold step and the number of generated test pulses (exposure window) are programmable.

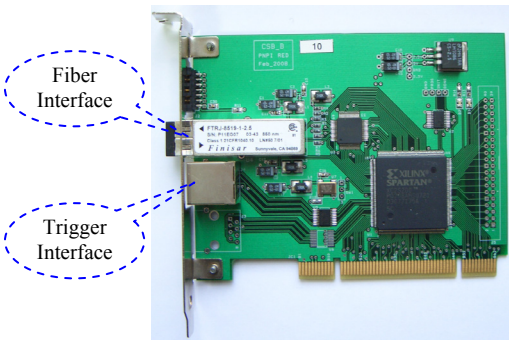


**Fig. 9.** CSB-B – the CROS-3B System Buffer

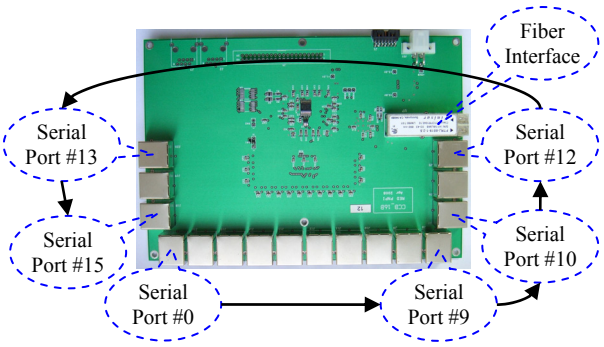


**Fig. 10.** CCB16-B – the CROS-3B Concentrator

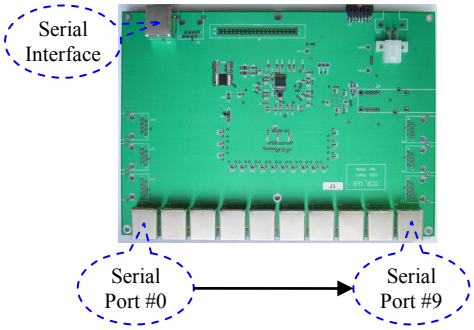


**Fig. 11.** CCB10-B – the CROS-3B Low-Level Concentrator

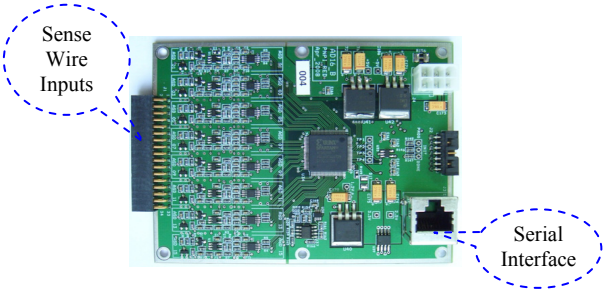


**Fig. 12.** AD16-B – the CROS-3B Digitizer

The CROS-3B command library provides an access to all CROS-3B registers. Examples of the system configuration and the data taking algorithms can be found in the CROS-3B Reference Guide [7]. A user is supposed to create his/her own code based on the above library and algorithms to effectively exploit all CROS-3B features.

## References


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