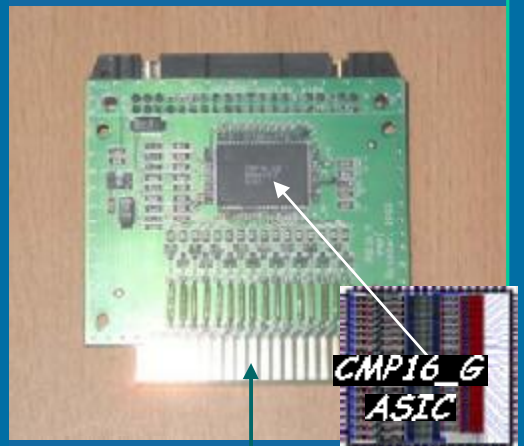
CROS3 Система Считывания



16_AD Board:
16-channel
Amplifier Shaper
Discriminator

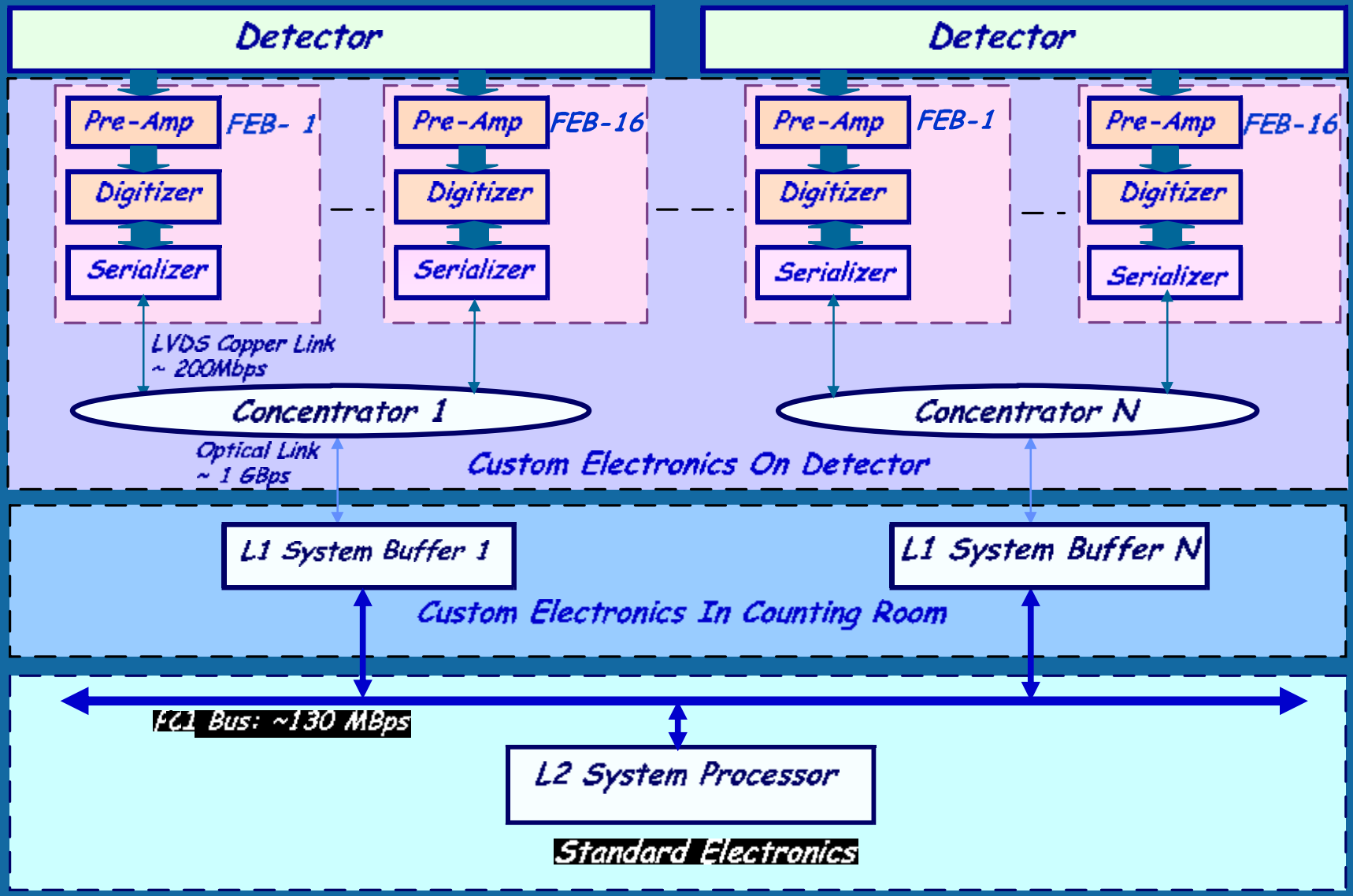
- Complete On-Chamber Multiwire Readout System
- Programmable Thresholds, Delays and Gates
- Time Distribution Measurement for Hit within Gate
- High Density, Low Power Packaging
- Interfaces to PCI and Ethernet
- Extremely Low Cost
- Two options of the system in progress:

CROS3_PWC – for Proportional Wire Chambers
CROS3_DC – for Drift Chamber

The System Specific Features:

Continuous digitization of the input data stream
Adjustable digital delay within 512 steps. The step ≤2.5 ns
Adjustable digital gate within 128 slices. The step ≤2.5 ns
LVDS signaling interconnect technology for short distance data path
Optical link technology for long distance data path
The core elements of the system are CMP16_G ASIC, ASDQ ASIC,
SPARTAN 3 FPGA XC3S200

CROS3 Структура



CROS3_PWC Структура