A HIGH SPEED READOUT SYSTEM FOR SILICON STRIP DETECTORS

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1. System Overview

The system being reported has been designed for SELEX (E781) — a high statistics study of charmed baryons in a fixed target experiment at Fermilab [1]. This design incorporates many lessons learned from operating a 12,000-strip SVX system [2] using the older SRS and SDA modules designed for early SVX studies by the Berkeley group (F.Kirsten, C.Haber). The total number of Si detector planes in the experiment is 44 with a total of 89,000 independent channels to be read out. The detectors are spread over a 10 meter distance along the beam. The electronic trigger rate is 10 kHz with 70% lifetime. The readout system logic diagram is shown in Figure below.

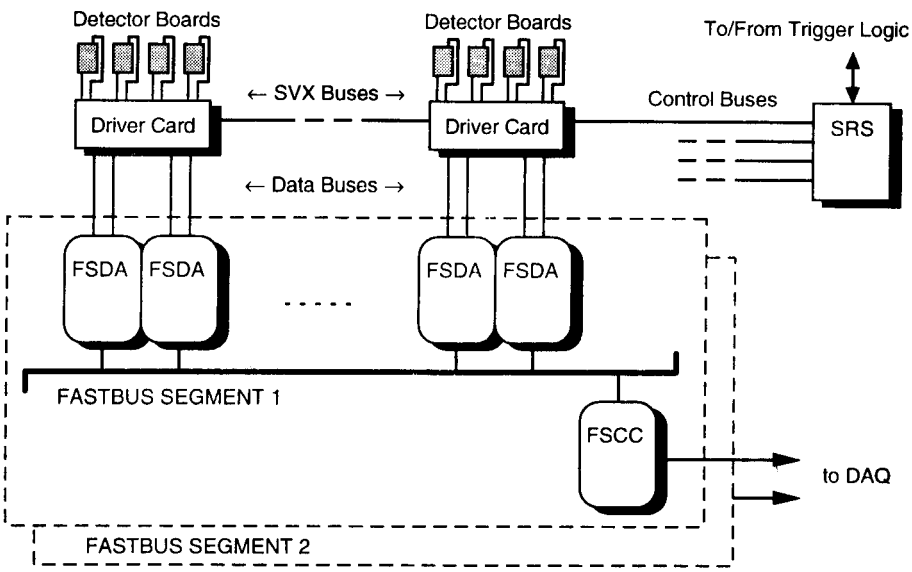

Fig. Silicon Strip Readout System logic diagram

There are two types of Detector Boards: Single-SVX-Bus Detector Boards with SVX chips mounted only on one edge of the Detector and Dual-SVX-Bus Detector Boards with SVX chips arranged across the opposite edges of the Si plane. In the latter case every other strip is wire-bonded to the SVX chip on the opposite SVX Bus. One of the SVX Buses provides data from all the even detector strips in ascending order while the other bus the data from all the odd strips in descending order.

The SVX Readout Sequencer (SRS) is a CAMAC module, which controls the data acquisition, reset, calibration and initial programming of all SVX chips in the system. The SRS has four Control Buses driven in parallel. Each Bus goes to a group of closely-spaced detectors, for which inter detector Control Bus delays are small compared to the Fermilab Tevatron RF period of 19 ns.

The major functions of the Driver Card are to fan-out SRS signals to each SVX Bus and to drive SVX signals to the FASTBUS SVX Digitizer & Accumulator (FSDA). Every SVX chip has its own threshold DAC located on the Driver Card. Each Driver Card serves up to eight Single-SVX-Bus Detector Boards or up to four Dual-SVX-Bus Detector Boards and drives up to two FSDA modules. There are 12 Driver Cards in the system to handle all 44 detectors.

The FSDA is the most complex component of the system. It is described in more detail in the section below. There are 19 FSDAs in the system arranged into two FASTBUS crates.

The FASTBUS Smart Crate Controller (FSCC) was designed at Fermilab. It has been chosen as a FASTBUS Master to readout the FSDAs in the system. The FSCC has a fast parallel output port to send the data being read out to the Data Acquisition System (DAQ).

2. FSDA

The FSDA is a single width FASTBUS module designed to collect and process Silicon Strip Detector data. One FSDA can collect data from either two silicon planes of Dual-SVX-Bus Detectors, or four planes of Single-SVX-Bus Detectors.

The FSDA receives both digital and analog data from SVX chips. The digital data are codes of hit strips, and the analog data are voltages proportional to the charges deposited on those strips. Below is a list of the module functions:

- Receives digital and analog data from the SVX chips;
- Converts the strip codes into logical strip numbers using a Lookup Memory;
- Checks correct (monotonic) order of logical strip numbers;
- Digitizes the analog data amplitudes;
- Subtracts preloaded pedestals individually for each strip from the digitized amplitudes;
- Suppresses data with amplitudes below pedestals;
- Suppresses data from designated "noisy" strips;
- Converts the amplitude codes into a four-bit format to fit each hit into two bytes;
- For Dual-SVX-Bus Detectors restores the ascending data order of the subplane with the odd strip codes and merges the data from two subplanes into a single list ordered by logical strip number;
- Forms headers for event data blocks, including event number and word count;
- FIFO buffers event data blocks to permit event building;
- Transmits the data to the FASTBUS backplane using MegaBlock mode;
- Detects and flags errors and data format corruption;

This functionality is implemented to reduce the bandwidth required for data transmission to a processor farm to an achievable level and to reduce the computation required for data preparation in the farm.

3. System Performance

The system performance was evaluated by a series of measurements on a 5×5 cm^2 AC-coupled Silicon Strip Detector. For the entire system the typical noise is 0.3 fC equivalent to a S/N ratio of 13/1, dominated by the detector contribution. By using a loop-back test, the noise intrinsic to the Driver Card and the FSDA combination was measured to be less than 0.06 fC. A single minimum ionizing particle deposits 4 fC.

Since the FSDA is FIFO buffered the detector readout rate and FASTBUS transfer rate may be different. The detector readout rate is limited by the SVX analog signal risetime to a 1.67 MHz (600 ns per channel). The Silicon Strip Readout System dead time with the expected detector occupancy is estimated as 21 μs, which is within the E781 requirements (30 μs). Data are transferred to FASTBUS at the rate of 250 ns per 32-bit word. For 10 kHz trigger rate (100 μs per event) 400 words are allowed per event in a crate segment.

The data processing functions performed by the FSDAs, if implemented in a computer, correspond to 100 MIPS per module of processing power. This system provides the speed and processing power to read out one of the world's largest silicon strip tracker at a 10 kHz rate.

REFERENCES

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PERFORMANCE OF FINE-MESH PHOTOMULTIPLIER TUBES PRODUCED IN RUSSIA

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Present and mainly future collider experiments on RHIC and LHC require the performance of photodetectors in strong magnetic fields, for example, in electromagnetic calorimeters in CMS, ALICE and TOF system in STAR (RHIC). Such detectors have to possess a good energy and time resolution, in TOF measurements less than 100ps, simultaneously being radiation hard up to absorbed doses of some Mrad. Fine mesh dynode proximity photomultiplier tubes (FMPMT) developed and produced in recent years by Hamamatsu are the